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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/772,936	02/05/2004	Yoshiyuki Ogata	85A 3501	6088
3713	7590	09/28/2005		
KODA & ANDROLIA			EXAMINER	
2029 CENTURY PARK EAST			DOLAN, JENNIFER M	
SUITE 1140				
LOS ANGELES, CA 90067			ART UNIT	PAPER NUMBER
			2813	

DATE MAILED: 09/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)
	10/772,936	OGATA ET AL.
	Examiner	Art Unit
	Jennifer M. Dolan	2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on ____.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-4 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) Claim(s) ____ is/are allowed.
- 6) Claim(s) 1-4 is/are rejected.
- 7) Claim(s) ____ is/are objected to.
- 8) Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 05 February 2004 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. ____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. ____. |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>2/5/04</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Publication No. 2003/0029033 to Hidese et al.

Regarding claims 1 and 4, Hidese discloses a method and apparatus for successively bonding chips (105) to a plurality of chip mount portions (102a) on a substrate (102), the method/apparatus including: a bonding step/bonding means that bonds a chip to a chip-mount portion by a bonding head (109; paragraphs 0040-0045); a bonding preparation step that moves the bonding head to a chip supplying portion (104, 106) to pick up a new chip (paragraphs 0037, 0040) and then moves the new chip to the chip mount portion (paragraph 0041); an imaging step/imaging means (using camera 115) performed in parallel with the bonding preparation step (paragraphs 0039-0040), the imaging step imaging chip-mount portions where bonding has already been performed (see paragraph 0045) and where bonding is going to be performed (paragraphs 0043-0044), the chip mount portions being contained in the same visual field thereof (see paragraphs 0031; 0045, 0052 – the entire board 102 is imaged in one step, the board containing portions already having a chip and portions where a chip is to be mounted); a position-detecting step that detects a position of the chip mount portion for position detection

based on acquired image data (paragraphs 0043-0044); and an inspection step that inspects a state of bonding of the chip-mount portions based on the acquired image data (paragraph 0045).

Regarding claims 2 and 3, Hidese discloses that the entire board is imaged, which would include imaging and detecting the chip-mount portions where bonding is to be performed next, or where bonding is to be performed after that (see paragraphs 0039-0045).

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 5,946,409 to Hori discloses a mounting apparatus wherein multiple chips or vacant chip portions are imaged in the same field of view at the chip-pick-up/chip supply location.

US 2001/0051394 to Kim et al, U.S. Patent No. 6,389,688 to Srivastava et al., and US 2003/0110623 to Haji et al. disclose a mounting apparatus/method wherein a plurality of cameras are used to ensure proper alignment between a chip and a mounting portion, but there is no post-mounting inspection step, and only a single chip is imaged in the field of view of the cameras.

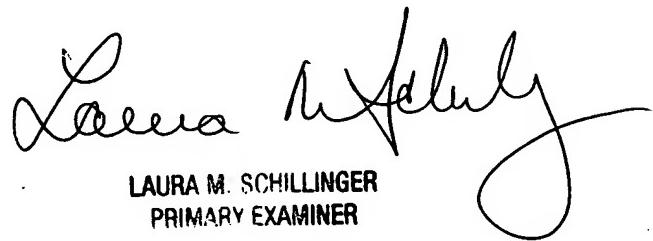
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd



LAURA M. SCHILLINGER
PRIMARY EXAMINER